disclosure. The input/output device **8712** may include at least one selected among a keypad, a keyboard, a display device, a touchscreen and so forth. The memory **8713** is a device for storing data. The memory **8713** may store data and/or commands to be executed by the controller **8711**, and the like.

The memory **8713** may include a volatile memory device such as a DRAM and/or a nonvolatile memory device such as a flash memory. For example, a flash memory may be mounted to an information processing system such as a mobile terminal or a desktop computer. The flash memory may constitute a solid state disk ("SSD"). In this case, the electronic system **8710** may stably store a large amount of data in a flash memory system.

The electronic system **8710** may further include an interface **8714** for transmitting and receiving data to and from a communication network. The interface **8714** may be a wired or wireless type. For example, the interface **8714** may include an antenna or a wired or wireless transceiver.

The electronic system **8710** may be realized as a mobile system, a personal computer, an industrial computer or a logic system performing various functions. For example, the mobile system may be any one of a personal digital assistant ("PDA"), a portable computer, a tablet computer, a mobile phone, a smart phone, a wireless phone, a laptop computer, a memory card, a digital music system and an information transmission/reception system.

If the electronic system **8710** is an equipment capable of performing wireless communication, the electronic system **8710** may be used in a communication system such as of Code Division Multiple Access ("CDMA"), Global System for Mobile communications ("GSM"), North American Digital Cellular ("NADC"), Enhanced-Time Division Multiple Access ("E-TDMA"), Wideband Code Division Multiple Access ("WCDAM"), CDMA2000, Long Term Evolution ("LTE") and Wireless Broadband Internet ("Wibro").

Embodiments of the present disclosure have been disclosed for illustrative purposes. Those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the present disclosure and the accompanying claims.

What is claimed is:

1. A semiconductor package comprising:

a substrate having a first surface and a second surface facing away from the first surface;

an elastic buffer layer disposed over the first surface of the substrate;

wiring patterns disposed on a first surface of the elastic buffer layer;

a semiconductor chip disposed on a second surface of the elastic buffer layer facing away from the first surface of the elastic buffer layer, wherein the semiconductor chip includes trenches formed on a surface facing the elastic buffer layer, wherein the elastic buffer layer crosses each trench to provide a respective cavity; and

interconnection members electrically connecting the wiring patterns to the substrate,

wherein each of the interconnection members has one end electrically connected to one of the wiring patterns and the other end electrically connected to the substrate.

2. A semiconductor package comprising:

a semiconductor chip (**400**) having a front-side portion (**400***a*) and a back-side portion (**400***b*) facing away from the front-side portion ;

a substrate (**300**) disposed under the front-side portion of the semiconductor chip;

an insulation layer (**420**) formed on the front-side portion of the semiconductor chip, wherein the insulation layer includes trenches (**431**) disposed therein and the trenches have a predetermined depth;

an elastic buffer layer (**445**) disposed between the insulation layer and the substrate, wherein the elastic buffer layer crosses each trench to provide a respective cavity (S**3**);

lower wiring patterns (**415**) disposed in the elastic buffer layer, wherein each of the lower wiring patterns includes a landing pad (**272**) aligned with one of the trenches; and

interconnection members (**312**) electrically connecting the landing pads to the substrate,

wherein each of the interconnection members has one end electrically connected to one of the landing pads and the other end electrically connected to the substrate.

3. The semiconductor package of claim **2**, wherein the elastic buffer layer includes:

a first elastic buffer layer disposed on a surface of the insulation layer facing away from the semiconductor chip and disposed to cover the trenches; and

a second elastic buffer layer disposed between the first elastic buffer layer and the substrate to cover the lower wiring patterns,

wherein the second elastic buffer layer includes openings exposing the landing pads.

4. The semiconductor package of claim **2**, wherein the insulation layer includes a plurality of insulation materials having different Young's moduli.

5. The semiconductor package of claim **4**,

wherein the insulation layer includes a first insulation material having a Young's modulus of about 2.9 GPa to about 3.2 GPa; and

wherein the elastic buffer layer includes a second insulation material having a Young's modulus of about 0.01 GPa to about 0.1 GPa.

6. The semiconductor package of claim **5**, wherein the first insulation material includes at least one selected from the group consisting of benzocyclobutene and polyimide.

7. The semiconductor package of claim **5**, wherein the second insulation material includes one or more of silicone resin and silicone rubber.

8. The semiconductor package of claim **2**,

wherein the insulation layer includes a first surface facing the elastic buffer layer and a second surface bonded to the semiconductor chip, and

wherein the trenches are spaced apart from each other and are adjacent to the first surface of the insulation layer.

9. The semiconductor package of claim **2**,

wherein the insulation layer further includes inner wiring patterns therein;

wherein each of the lower wiring patterns comprising the landing pads is connected to one of the inner wiring patterns at least at one surface; and

wherein the inner wiring patterns are in contact with and connected to chip pads disposed on the front-side portion of the semiconductor chip to electrically connect the chip pads to the lower wiring patterns.

10. The semiconductor package of claim **2**, wherein the remaining portions of the lower wiring patterns except for the landing pads are covered with the elastic buffer layer.

11. The semiconductor package of claim **2**, wherein the landing pad is spaced apart from a bottom surface of the trench aligned with the landing pad by a predetermined distance.